METHOD AND MANUFACTURE OF THIN SILICON ON INSULATOR (SOI) WITH RECESSED CHANNEL AND DEVICES MANUFACTURED THEREBY

BACKGROUND OF INVENTION

[0001] This invention relates to methods of manufacture of SOI (Silicon-On-Insulator) MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices and more particularly to UT (Ultra-Thin) RSD (Raised Source and Drain) devices and to the structures manufactured thereby.

[0002] Thin silicon channel SOI device technology is a promising option for continued scaling of the manufacture of SOI CMOS devices to smaller and smaller dimensions. It has the advantage of sharper sub-threshold slope, high mobility (since the devices are operated at a lower effective field), low junction capacitance, elimination of CMOS latch-up, and better short-channel effect control. The disadvantage of such devices is that the series resistance increases as the SOI film is thinned. One solution to the series resistance problem is the use of an elevated source drain that may be created by selective epitaxial Si growth.

[0003] In some prior art thin Si channel devices, extensions are implanted prior to RSD formation. This causes at least two problems. A first problem is that since that a PMOS FET extension requires a fairly thick offset spacer, a high resistance region exists under the spacer. The second problem is that since extension implants are performed prior to the RSD process, the dopants are subjected to the significant thermal budget of the RSD process. This can cause unwanted diffusion of the dopants. In addition, the incubation time is different for P type silicon and N type silicon which leads to substantially different RSD thickness for PMOS FET and NMOS FET devices. Also, the surface concentration of the dopants must be uniform across the wafer as well as from wafer to wafer, which is a major challenge, if the RSD process is to be manufacturable.

[0004] In another prior art thin silicon (Si) channel device, a disposable spacer process is used. A wide disposable spacer is used to grow the RSD. Next, deep source and drain implants are performed. Then the spacer is removed, and the extensions are implanted. Although the disposable spacer scheme overcomes the problem of subjecting the extensions to the RSD thermal budget, that process does not overcome the problem of the high resistance region outside the RSD layer. Based upon the above remarks, it is clear that a need exists for a way to overcome the high resistance problem as well as the thermal budget problem.

[0005] U.S. Pat. No. 6,465,311 of Shenoy entitled "Method of Making a MOSFET Structure Having Improved Source/ Drain Junction Performance" describes a MOSFET structure including a gate stack formed over a gate oxide above an active region of a substrate. With a pair of shallow trenches defined on either side of the gate stack, an intrinsic silicon material is disposed within the pair of shallow trenches up to a top surface of the gate stack. The MOSFET structure includes source and drain implanted impurities that are defined in an upper portion of the intrinsic silicon material. The upper portion is configured to extend down into the intrinsic silicon material to a target diffusion level that is just below the gate oxide of the gate stack.

[0006] U.S. Pat. No. 6,391,720 of Sneelal et al. entitled "Process Flow For A Performance Enhanced MOSFET with Self-Aligned, Recessed Channel" describes forming a self-recessed channel, MOSFET. A patterned mask oxide layer is formed over a substrate with an active area encompassed by a shallow trench isolation (STI) region. Then the surface and a portion of the STI region are etched. Next the mask oxide layer is removed. In the unmasked area a gate recess is created. Then a thin pad oxide layer is grown on the surface and a thick silicon nitride layer is formed covering the surface and filling the gate recess. Top surface planarization exposes the pad oxide layer. Growth of an additional oxide layer thickens the pad oxide layer. A portion of the silicon nitride layer is etched away. An additional oxide layer is grown further thickening the pad oxide layer to form a tapered oxide layer along the sidewalls of the gate recess. Then the remaining silicon nitride layer is removed, rethe gate recess. A threshold adjust and punchimplantation is performed into the substrate below the gate recess. Then isotropic etching of the pad oxide removes the oxide layer at the bottom of the gate recess. A gate dielectric layer is grown in the bottom of the gate recess. Then gate polysilicon is deposited over the top surface, filling the gate recess. The top surface is replanarized to expose the substrate. Then a screen oxide layer is deposited, followed by light and heavy S/D implantations and annealing. Metallization and passivation complete the fabrication of the MOS transistor device.

[0007] U.S. Pat. No. 6,225,173 of Yu entitled "Recessed Channel Structure For Manufacturing Shallow Source/Drain Extensions" describes a method of fabricating integrated circuit CMOS FET devices with ultrasource and drain junctions utilizing a damascene process. The substrate is overto form extensions in the source and drain regions.

[0008] U.S. Pat. No. 5,814,544 of Huang entitled "Forming a MOS Transistor with A Recessed Channel" describes fabrication of a MOS transistor by forming an inverse gate mask consisting of a lower silicon dioxide layer and an upper silicon nitride layer. The exposed channel region is thermally oxidized. The mask is removed to permit a source/drain implant. The thermal oxide is removed so that the channel region is recessed. A differential oxide growth then serves to mask the source and the drain for channel threshold adjust and punchimplants. A doped polysilicon gate is formed, with the thinner area of the differential oxide serving as the gate oxide. In the resulting structure, the punchthrough dopant is spaced from the source and the drain, reducing parasitic capacitance and improving transistor switching speeds.

[0009] U.S. Pat. No. 4,616,400 of Macksey et al. entitled "Process for Fabricating A Double Recess Channel Field Effect Transistor" forming a double recess, N+ ledge FET using a single masking step. Two layers of photoresist of differing types are formed on the surface of an N+ epitaxial layer. A layer of material that may be etched by RIE with Freon®, but will not etch by RIE with oxygen, is formed over the photoresist layers. A gate pattern is etched into this surface layer of material and the photoresist layers are selectively undercut to provide a pattern to etch the gate recess and the wide recess. A gate contact is then formed by perpendicular evaporation through the gate pattern in the surface layer of material. A process is provided for forming a selfdouble recess transistor using a single mask to form the